AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Previously Presented) A comparator comprising:

a first input transistor with a first terminal, a second terminal and a gate terminal, wherein the gate terminal is in communication with a first input and the first terminal of the first input transistor is in communication with a first reference voltage via a first electrical path, the first electrical path including a first current source and a resistor to generate a hysteresis offset;

a second input transistor with a first terminal, a second terminal and a gate terminal, wherein the gate terminal is in communication with a second input and the first terminal of the second input transistor is in communication with the first reference voltage via a second electrical path;

a third transistor having a first terminal, a second terminal and a gate terminal, wherein the gate terminal communicates with said second terminal of said first input transistor;

a capacitor that communicates with said gate of said third transistor; and

an output setting toward the first reference voltage when a first signal at the first input exceeds the hysteresis offset or a second reference voltage when the first signal at the first input does not exceed the hysteresis offset.

2. (Previously Presented) A comparator as in claim 1, wherein the hysteresis offset is controllable.

3. (Previously Presented) A comparator as in claim 2, wherein the amount of current generated by the current source is controllable, thereby affecting the hysteresis offset.

4. (Cancelled).

5. (Previously Presented) A comparator as in claim [4]1, wherein the first terminal of the third transistor is in communication with the first reference voltage via a third electrical path, the third electrical path including a current source.

6. (Original) A comparator as in claim 5, wherein the output of the comparator is located along the third electrical path between the first terminal of the third transistor and the current source.

7. (Cancelled).

8. (Currently Amended) A comparator as in claim 1~~, wherein the hysteresis delay circuit includes~~ further comprising a switch that communicates with the capacitor.

9. (Cancelled).

10. (Previously Presented) A device comprising:

a first programmable circuit operable to selectively provide a hysteresis offset in response to a first programmable control signal;

a comparator circuit, responsive to the first programmable circuit, to receive a first and a second signals and compare the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the comparator circuit provides a digital output signal in response to result of comparison; and

a second programmable circuit in communication with the comparator circuit and operable to selectively provide a hysteresis delay in response to a second programmable control signal, wherein the comparator circuit compares the first signal and the second signal with applying the hysteresis delay.

11. (Previously Presented) The device of claim 10, wherein the device is programmable by a user for boundary-scan testing.

12. (Previously Presented) The device of claim 10, wherein the first and second input signals are mixed signals.

13. (Currently Amended) The device of claim 10, wherein the first programmable circuit includes a programmable impedance element for selectively setting the hysteresis offset in response to ~~a~~ the first programmable ~~circuit~~ control signal.

14. (Currently Amended) The device of claim 10, wherein the first programmable circuit includes a programmable current source for selectively setting minimal voltage for input signals in response to ~~a~~ the first programmable ~~circuit~~ control signal.

15. (Original) The device of claim 14, wherein the programmable current source includes a plurality of selectable current sources.

16. (Original) The device of claim 10, wherein the second programmable circuit includes programmable capacitance element, wherein the programmable capacitance element selectively sets hysteresis delay for input signals.

17. (Original) The device of claim 16, wherein the programmable capacitance element includes a plurality of selectable capacitors and switchers, wherein the switchers is operable to receive second programmable control signals.

18. (Currently Amended) A device comprising:

a first programmable circuit operable to selectively provide a hysteresis offset in response to a first programmable control signal;

a comparator circuit, responsive to the first programmable circuit, to receive a first and a second signals and compare the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the comparator circuit provides a digital output signal in response to result of comparison; and

a ~~third~~ second programmable circuit in communication with the comparator circuit and operable to selectively provide control of magnitude of the digital output signal.

19. (Currently Amended) The device of claim 18, wherein the ~~third~~ second programmable circuit further includes a plurality of selectable current sources.

20. (Currently Amended) A device comprising:

a first programmable circuit operable to selectively provide a hysteresis offset in response to a first programmable control signal;

a comparator circuit, responsive to the first programmable circuit, to receive a first and a second signals and compare the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the

comparator circuit provides a digital output signal in response to result of comparison; and

a ~~third~~ second programmable circuit in communication with the first programmable circuit and operable to program an output current source for facilitating the digital output signal.

21. (Cancelled).

22. (Previously Presented) A device comprising:

means for selectively providing a hysteresis offset in response to a first programmable control signal;

means for receiving a first and a second signals;

means for comparing the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the means for comparing further includes means for providing a digital output signal in response to result of comparison; and

means for selectively providing a hysteresis delay in response to a second programmable control signal, wherein the means for comparing further includes means for comparing the first signal and the second signal with applying the hysteresis delay the second signal.

23. (Previously Presented) The device of claim 22, wherein the device includes means for receiving programmable information from a user for boundary-scan testing.

24. (Previously Presented) The device of claim 22, wherein the means for receiving a first and a second signals further includes means for receiving mixed signals.

25. (Currently Amended) The device of claim 22, wherein the means for selectively providing a hysteresis offset further includes means for selecting an impedance in response to the first programmable ~~circuit~~ control signal.

26. (Currently Amended) The device of claim 22, wherein the means for selectively providing a hysteresis offset further includes means for selectively providing a programmable current source for setting minimal voltage for input signals in response to the first programmable ~~circuit~~ control signal.

27. (Original) The device of claim 26, wherein the means for providing a programmable current source includes means for providing a plurality of selectable current sources.

28. (Original) The device of claim 22, wherein the means for selectively providing a hysteresis delay further includes means for selectively setting capacitance in response to the second programmable control signal.

29. (Original) The device of claim 28, wherein the means for selectively setting capacitance further includes means for activating one capacitor or a combination of a plurality of selectable capacitors.

30. (Previously Presented) A device comprising:

means for selectively providing a hysteresis offset in response to a first programmable control signal;

means for receiving a first and a second signals;

means for comparing the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the means for comparing further includes means for providing a digital output signal in response to result of comparison; and

means for selectively providing control to magnitude of the digital output signal.

31. (Original) The device of claim 30, wherein the means for selectively providing control to magnitude of the digital output signal includes means for selecting one current source or a combination of a plurality of selectable current sources.

32. (Previously Presented) A device comprising:

means for selectively providing a hysteresis offset in response to a first programmable control signal;

means for receiving a first and a second signals;

means for comparing the first signal and the second signal with applying the hysteresis offset to the second signal, wherein the means for comparing further includes means for providing a digital output signal in response to result of comparison; and

means for programming an output current source for facilitating the digital output signal.

33. (Cancelled).

34. (Previously Presented) A method for operating a comparator comprising:

a) receiving first programmable control information;

b) setting a hysteresis offset in response to the first programmable control information;

c) receiving a first and a second input signals;

d) offsetting the second input signal with the hysteresis offset;

e) comparing the first input signal with the signal in step (d);

f) receiving second programmable control information;

g) setting a hysteresis delay in response to the second programmable control information;

h) adjusting the second input signal in response to the hysteresis delay; and

i) comparing the first input signal with the adjusted second input signal.

35. (Previously Presented) The method of claim 34, wherein the method includes receiving first programmable control information from a user.

36. (Previously Presented) The method of claim 34, wherein receiving a first and a second input signals further includes receiving mixed signals.

37. (Currently Amended) The method of claim 34, wherein setting a hysteresis offset further includes selecting an impedance in response to the first programmable ~~circuit~~ control ~~signal~~information.

38. (Currently Amended) The method of claim 34, wherein setting a hysteresis offset further includes providing a programmable current source for selectively setting minimal voltage for input signals in response to the first programmable ~~circuit~~ control ~~signal~~ information.

39. (Original) The method of claim 38, wherein the a programmable current source includes providing a plurality of selectable current sources.

40. (Currently Amended) The method of claim 34, wherein setting a hysteresis delay further includes selectively setting capacitance in response to the second programmable control ~~signal~~information.

41. (Original) The method of claim 40, wherein the selectively setting capacitance further includes activating one capacitor or a combination of a plurality of selectable capacitors.

42. (Previously Presented) A method for operating a comparator comprising:

a) receiving first programmable control information;

b) setting a hysteresis offset in response to the first programmable control information;

c) receiving a first and a second input signals;

d) offsetting the second input signal with the hysteresis offset;

e) comparing the first input signal with the signal in step (d); and

f) selectively providing control to magnitude of the digital output signal.

43. (Original) The method of claim 42, wherein the selectively providing control to magnitude of the digital output signal includes selecting one current source or a combination of a plurality of selectable current sources.

44. (Previously Presented) A method for a comparator comprising:

a) receiving first programmable control information;

b) setting a hysteresis offset in response to the first programmable control information;

c) receiving a first and a second input signals;

d) offsetting the second input signal with the hysteresis offset;

e) comparing the first input signal with the signal in step (d); and

f) programming an output current source for facilitating the digital output signal.

45. (Cancelled).

46. (Previously Presented) A programmable comparator comprising:

a first programmable circuit operable to selectively provide a hysteresis delay in response to a first programmable control signal;

a comparator circuit, responsive to the first programmable circuit, to receive a first and a second input signals in response to the hysteresis delay and

provide a digital output signal in response to result of comparison between the first and second input signals; and

a second programmable circuit in communication with the comparator circuit and operable to selectively provide a hysteresis offset in response to a second programmable control signal, wherein the comparator circuit receives the first input signal and the second input signal in response to the hysteresis offset.

47. (Previously Presented) The programmable comparator of claim 46, wherein the programmable comparator is programmable by a user.

48. (Previously Presented) The programmable comparator of claim 46, wherein the first and second input signals are mixed signals.

49. (Currently Amended) The programmable comparator of claim 46, wherein the second programmable circuit includes a programmable impedance element for selectively setting the hysteresis offset in response to ~~a~~ the second programmable ~~circuit~~ control signal.

50. (Original) The programmable comparator of claim 46, wherein the second programmable circuit includes a programmable current source for selectively setting minimal voltage for input signals in response to a first programmable circuit control signal .

51. (Original) The programmable of claim 50, wherein the programmable current source includes a plurality of selectable current sources.

52. (Currently Amended) The programmable comparator of claim 46, wherein the first programmable circuit includes programmable capacitance element, wherein the programmable capacitance element selectively sets the hysteresis delay for input signals based on said first programmable control signal~~s~~.

53. (Currently Amended) The programmable comparator of claim 52, wherein the programmable capacitance element includes a plurality of selectable capacitors and switchers, wherein the switchers is operable to receive said first programmable control signal~~s~~.

54. (Original) The programmable comparator of claim 46 further comprising a third programmable circuit in communication with the comparator circuit and operable to selectively provide control to magnitude of the digital output signal.

55. (Original) The programmable comparator of claim 54, wherein the third programmable circuit further includes a plurality of selectable current sources.

56. (Original) The programmable comparator of claim 46 further comprising a third programmable circuit in communication with the comparator circuit and operable to programming an output transistor for facilitating the digital output signal.

57. (Cancelled).

58. (Previously Presented) A programmable apparatus comprising:

means for selectively providing a hysteresis delay in response to a first programmable control signal;

means for receiving a first and a second input signals in response to the hysteresis delay;

means for comparing the first and second input signals and providing a digital output signal in response to result of comparison between the first and second input signals; and

means for selectively providing a hysteresis offset in response to a second programmable control signal, wherein the means for receiving a first and a second input signals further includes means for receiving the first input signal and the second input signal in response to the hysteresis offset.

59. (Original) The programmable apparatus of claim 58 further includes means for receiving the first and second programmable control signals from a user.

60. (Previously Presented) The programmable apparatus of claim 58, wherein the means for receiving a first and a second input signals further includes means for receiving mixed signals.

61. (Currently Amended) The programmable apparatus of claim 58, wherein means for selectively providing a hysteresis offset includes means for selectively setting the hysteresis offset in response to ~~a~~ the second programmable ~~circuit~~ control signal.

62. (Currently Amended) The programmable apparatus of claim 58, wherein means for selectively providing a hysteresis offset further includes means for selectively setting minimal voltage for input signals in response to ~~a~~ the first programmable ~~circuit~~ control signal.

63. (Original) The programmable apparatus of claim 62, wherein means for selectively setting minimal voltage for input signals further includes means for providing a plurality of selectable current sources.

64. (Previously Presented) The programmable apparatus of claim 58, wherein means for selectively providing a hysteresis delay includes means for selectively setting capacitance in response to the first programmable control signal.

65. (Original) The programmable apparatus of claim 64, wherein means for selectively setting capacitance includes means for selecting one capacitor or a combination of a plurality of selectable capacitors.

66. (Original) The programmable apparatus of claim 58 further comprising means for selectively providing control to magnitude of the digital output signal.

67. (Original) The programmable apparatus of claim 66, wherein means for selectively providing control to magnitude of the digital output signal further includes means for selecting one current source or a combination of a plurality of selectable current sources.

68. (Original) The programmable apparatus of claim 58 further comprising means for programming an output current source for facilitating the digital output signal.

69. (Cancelled).

70. (Previously Presented) A method for comparing input signals comprising:

a) providing a hysteresis delay in response to a first programmable control signal;

b) receiving a first and a second input signals in response to the hysteresis delay;

c) comparing the first and second input signals;

d) providing a digital output signal in response to result of comparison between the first and second input signals; and

e) providing a hysteresis offset in response to a second programmable control signal, wherein the receiving a first and a second input signals further includes receiving the first input signal and the second input signal in response to the hysteresis offset.

71. (Original) The method of claim 70 further includes receiving the first and second programmable control signals from a user.

72. (Cancelled).

73. (Currently Amended) ~~The method of Claim 70,~~A method for comparing input signals comprising:

a) providing a hysteresis delay in response to a first programmable control signal;

b) receiving a first and a second input signals in response to the hysteresis delay;

c) comparing the first and second input signals; and

d) providing a digital output signal in response to result of comparison between the first and second input signals, wherein the receiving a first and a second input signals further includes receiving signals, wherein the selectively providing a hysteresis offset includes selectively setting the hysteresis offset in response to ~~a~~ the second programmable ~~circuit~~ control signal.

74. (Currently Amended) The method of claim 70, wherein the selectively providing a hysteresis offset further includes selectively setting minimal voltage for input signals in response to ~~a~~ the first programmable ~~circuit~~ control signal~~-~~.

75. (Original) The method of claim 74, wherein the selectively setting minimal voltage for input signals further includes providing a plurality of selectable current sources.

76. (Previously Presented) The method of claim 70, wherein the selectively providing a hysteresis delay includes selectively setting capacitance in response to the first programmable control signal.

77. (Original) The method of claim 76, wherein the selectively setting capacitance includes selecting one capacitor or a combination of a plurality of selectable capacitors.

78. (Original) The method of claim 70 further comprising the selectively providing control of magnitude of the digital output signal.

79. (Original) The method of claim 78, wherein the selectively providing control of magnitude of the digital output signal further includes selecting one current source or a combination of a plurality of selectable current sources.

80. (Original) The method of claim 70 further comprising programming an output current source for facilitating the digital output signal.

81. (Cancelled).

82. (Previously Presented) A device comprising:

a first programmable circuit operable to selectively providing an output loading on an output circuit in response to a first programmable control signal;

a comparator circuit in communication with the first programmable circuit to compare a first input signal and a second input signal and provide a digital output signal in response to result of comparison and the output loading on the output circuit: and

a second programmable circuit operable to selectively provide a hysteresis offset in response to a second programmable control signal, wherein

the comparator circuit receives the first and the second input signals with applying the hysteresis offset.

83. (Currently Amended) A device comprising:

a first programmable circuit operable to selectively providing an output loading on an output circuit in response to a first programmable control signal;

a comparator circuit in communication with the first programmable circuit to compare a first input signal and a second input signal and provide a digital output signal in response to result of comparison and the output loading on the output circuit: and

a ~~third~~ second programmable circuit in communication with the comparator circuit and operable to selectively provide a hysteresis delay in response to a third programmable control signal, wherein the comparator circuit receives the first signal and the second signal with applying the hysteresis delay.

84. (Previously Presented) The device of claim 82, wherein the device is programmable by a user.

85. (Previously Presented) The device of claim 82, wherein the first and second input signals are mixed signals.

86. (Currently Amended) The device of claim 82, wherein the second programmable circuit includes a programmable impedance element for selectively setting the hysteresis offset in response to ~~a~~ the first programmable ~~circuit~~ control signal.

87. (Currently Amended) The device of claim 82, wherein the second programmable circuit includes a programmable current source for selectively setting minimal voltage for input signals in response to ~~a~~ the first programmable ~~circuit~~ control signal.

88. (Original) The device of claim 87, wherein the programmable current source includes a plurality of selectable current sources.

89. (Original) The device of claim 83, wherein the third programmable circuit includes programmable capacitance element, wherein the programmable capacitance element selectively sets hysteresis delay for input signals.

90. (Original) The device of claim 89, wherein the programmable capacitance element includes a plurality of selectable capacitors and switchers, wherein the switchers is operable to receive second programmable control signals.

91. (Previously Presented) The device of claim 82, wherein the first programmable circuit selectively controls magnitude of the digital output signal.

92. (Original) The device of claim 91, wherein the first programmable circuit further includes a plurality of selectable current sources.

93. (Cancelled).

94. (Previously Presented) A device comprising:

means for selectively providing an output loading on an output circuit in response to a first programmable control signal;

means for comparing a first input signal and a second input signal and providing a digital output signal in response to result of comparison and the output loading on the output circuit; and

means for selectively providing a hysteresis offset in response to a second programmable control signal, wherein means for comparing further includes means for receiving the first and the second input signals with applying the hysteresis offset.

95. (Currently Amended) A device comprising:

means for selectively providing an output loading on an output circuit in response to a first programmable control signal;

means for comparing a first input signal and a second input signal and providing a digital output signal in response to result of comparison and the output loading on the output circuit; and

means for selectively providing a hysteresis delay in response to a ~~third~~ second programmable control signal, wherein means for comparing further includes means for receiving the first signal and the second signal with applying the hysteresis delay.

96. (Currently Amended) The device of claim 94 further includes means for receiving the first~~,~~ and second ~~and third~~ programmable control signals from a user.

97. (Previously Presented) The device of claim 94, wherein means for receiving the first and second input signals further includes means for receiving mixed signals.

98. (Currently Amended) The device of claim 94, wherein means for selectively providing a hysteresis offset further includes means for selectively providing an impedance for setting the hysteresis offset in response to ~~a~~ the first programmable ~~circuit~~ control signal.

99. (Original) The device of claim 94, wherein means for selectively providing a hysteresis offset includes means for providing a programmable current source for selectively setting minimal voltage for input signals.

100. (Original) The device of claim 99, wherein means for providing a programmable current source includes means for providing a plurality of selectable current sources.

101. (Original) The device of claim 95, wherein means for selectively providing a hysteresis delay further includes means for selectively setting capacitance in response to the third programmable control signal.

102. (Original) The device of claim 101, wherein means for selectively setting capacitance further includes means for activating one capacitor or a combination of a plurality of selectable capacitors.

103. (Previously Presented) The device of claim 94, wherein means for selectively providing an output loading further includes means for selectively controlling magnitude of the digital output signal.

104. (Original) The device of claim 103, wherein means for selectively controlling magnitude of the digital output signal includes means for selecting one or a combination of a plurality of selectable current sources.

105. (Cancelled).

106. (Previously Presented) A method for performing a compare function comprising:

selectively providing an output loading on an output circuit in response to a first programmable control signal;

comparing a first input signal and a second input signal and providing a digital output signal in response to result of comparison and the output loading on the output circuit; and

selectively providing a hysteresis offset in response to a second programmable control signal, wherein the comparing further includes receiving the first and the second input signals with applying the hysteresis offset.

107. (Currently Amended) A method for performing a compare function comprising:

selectively providing an output loading on an output circuit in response to a first programmable control signal;

comparing a first input signal and a second input signal and providing a digital output signal in response to result of comparison and the output loading on the output circuit; and

selectively providing a hysteresis delay in response to a ~~third~~ second programmable control signal, wherein the comparing further includes receiving the first signal and the second signal with applying the hysteresis delay.

108. (Currently Amended) The method of claim 106 further includes receiving the first~~,~~ and second ~~and third~~ programmable control signals from a user.

109. (Previously Presented) The method of claim 106, wherein the receiving the first and second input signals further includes receiving mixed signals.

110. (Currently Amended) The method of claim 106, wherein the selectively providing a hysteresis offset further includes selectively providing an impedance for setting the hysteresis offset in response to ~~a~~ the first programmable ~~circuit~~ control signal.

111. (Original) The method of claim 106, wherein the selectively providing a hysteresis offset includes providing a programmable current source for selectively setting minimal voltage for input signals.

112. (Original) The method of claim 111, wherein the providing a programmable current source further includes providing a plurality of selectable current sources.

113. (Original) The method of claim 107, wherein the selectively providing a hysteresis delay further includes selectively setting capacitance in response to the third programmable control signal.

114. (Original) The method of claim 113, wherein the selectively setting capacitance further includes activating one capacitor or a combination of a plurality of selectable capacitors.

115. (Previously Presented) The method of claim 106, wherein the selectively providing an output loading further includes selectively controlling magnitude of the digital output signal.

116. (Original) The method of claim 115, wherein the selectively controlling magnitude of the digital output signal includes selecting one or a combination of a plurality of selectable current sources.

117. (Previously Presented) A device comprising:

a hysteresis offset circuit that generates a hysteresis offset;

a hysteresis delay circuit that generates a hysteresis delay; and

a comparator circuit that receives first and second input signals and communicates with said hysteresis offset circuit and said hysteresis delay circuit, that generates a first output signal when said first input signal exceeds said second input signal plus said hysteresis offset for a period greater than said hysteresis delay, and

that generates a second output signal when at least one of said first input signal does not exceed said second input signal plus said hysteresis offset and/or when said first input signal does not exceed said second input signal plus said hysteresis offset for said period.

118. (Previously Presented) The device of Claim 117 wherein said comparator circuit includes an output circuit and further comprising an output loading circuit that communicates with said output circuit and that adjusts output loading of said output circuit.

119. (Previously Presented) A device comprising:

a hysteresis offset circuit that generates a hysteresis offset;

an output loading circuit that generates an output loading adjustment; and

a comparator circuit that receives first and second input signals, communicates with said hysteresis offset circuit and includes an output circuit that communicates with said output loading circuit, that generates one of a first output signal or a second output signal based on said first input signal, said second input signal, said hysteresis offset and said output loading adjustment.

120. (Previously Presented) The device of Claim 119 further comprising a hysteresis delay circuit that generates a hysteresis delay, wherein said comparator circuit generates one of said first or second output signals based on said first input

signal, said second input signal, said hysteresis offset, said output loading adjustment and said hysteresis delay.

121. (Previously Presented) A device comprising:

a hysteresis delay circuit that generates a hysteresis delay;

an output loading circuit that generates an output loading adjustment; and

a comparator circuit that receives first and second input signals, communicates with said hysteresis delay circuit and includes an output circuit that communicates with said output loading circuit, that generates one of a first output signal or a second output signal based on said first input signal, said second input signal, said hysteresis delay and said output loading adjustment.

122. (Previously Presented) The device of Claim 121 further comprising a hysteresis offset circuit that generates a hysteresis offset, wherein said comparator circuit generates one of said first or second output signals based on said first input signal, said second input signal, said hysteresis delay, said output loading adjustment and said hysteresis offset.

123. (Previously Presented) A device comprising:

a hysteresis offset circuit that generates a hysteresis offset;

a hysteresis delay circuit that generates a hysteresis delay; and

a comparator circuit that receives first and second input signals and communicates with said hysteresis offset circuit and said hysteresis delay circuit, that

generates one of a first output signal or a second output signal based on said first input signal, said second input signal, said hysteresis offset and said hysteresis delay.

124. (Previously Presented) The device of Claim 123 wherein said comparator circuit includes an output circuit and further comprising an output loading circuit that generates an output loading adjustment, wherein said comparator circuit generates one of said first or second output signals based on said first input signal, said second input signal, said hysteresis offset, said hysteresis delay and said output loading adjustment.

125. (Previously Presented) A device comprising:

hysteresis offset means for generating a hysteresis offset;

hysteresis delay means, for generating a hysteresis delay; and

comparator means that receives first and second input signals and communicates with said hysteresis offset means and said hysteresis delay means, for generating a first output signal when said first input signal exceeds said second input signal plus said hysteresis offset for a period greater than said hysteresis delay, and for generating a second output signal when at least one of said first input signal does not exceed said second input signal plus said hysteresis offset and/or when said first input signal does not exceed said second input signal plus said hysteresis offset for said period.

126. (Previously Presented) The device of Claim 125 wherein said comparator means includes output means for outputting one of said first or second output signals based on an output loading adjustment and further comprising output loading means that generates said output loading adjustment.

127. (Previously Presented) A device comprising:

hysteresis offset means for generating a hysteresis offset;

output loading means for generating an output loading adjustment; and

comparator means, that receives first and second input signals, communicates with said hysteresis offset means and includes output means that communicates with said output loading means, for generating one of a first output signal or a second output signal based on said first input signal, said second input signal, said hysteresis offset and said output loading adjustment.

128. (Previously Presented) The device of Claim 127 further comprising hysteresis delay means for generating a hysteresis delay, wherein said comparator means generates one of said first or second output signals based on said first input signal, said second input signal, said hysteresis offset, said output loading adjustment and said hysteresis delay.

129. (Previously Presented) A device comprising:

hysteresis delay means for generating a hysteresis delay;

output loading means for generating an output loading adjustment; and

comparator means, that receives first and second input signals, communicates with said hysteresis delay means and includes output means that communicates with said output loading means, for generating one of a first output signal or a second output signal based on said first input signal, said second input signal, said hysteresis delay and said output loading adjustment.

130. (Previously Presented) The device of Claim 129 further comprising hysteresis offset means for generating a hysteresis offset, wherein said comparator means generates one of said first or second output signals based on said first input signal, said second input signal, said hysteresis delay, said output loading adjustment and said hysteresis offset.

131. (Previously Presented) A device comprising:

hysteresis offset means for generating a hysteresis offset;

hysteresis delay means for generating a hysteresis delay; and

comparator means, that receives first and second input signals and communicates with said hysteresis offset means and said hysteresis delay means, for generating one of a first output signal or a second output signal based on said first input signal, said second input signal, said hysteresis offset and said hysteresis delay.

132. (Previously Presented) The device of Claim 131 wherein said comparator means includes output means for outputting said first output signal or said second output signal based on an output loading adjustment and further comprising

output loading means for generating said output loading adjustment, wherein said comparator means generates one of said first or second output signals based on said first input signal, said second input signal, said hysteresis offset, said hysteresis delay and said output loading adjustment.

133. (Previously Presented) A method comprising:

generating a hysteresis offset;

generating a hysteresis delay;

generating a first output signal when said first input signal exceeds said second input signal plus said hysteresis offset for a period greater than or equal to said hysteresis delay; and

generating a second output signal when at least one of said first input signal does not exceed said second input signal plus said hysteresis offset and/or when said first input signal does not exceed said second input signal plus said hysteresis offset for said period.

134. (Previously Presented) The method of Claim 133 further comprising adjusting output loading.

135. (Currently Amended) A method comprising:

setting a hysteresis offset;

setting an output loading adjustment; and

generating one of a first output signal or a second output signal based on ~~said~~ a first input signal, ~~said~~ a second input signal, said hysteresis offset and said output loading adjustment.

136. (Currently Amended) The method of Claim 135 further comprising:

setting a hysteresis delay; and

generating one of said first or second output signals based on ~~said~~ a first input signal, ~~said~~ a second input signal, said hysteresis offset, said output loading adjustment and said hysteresis delay.

137. (Currently Amended) A method comprising:

setting a hysteresis delay;

setting an output loading adjustment; and

generating one of a first output signal or a second output signal based on ~~said~~ a first input signal, ~~said~~ a second input signal, said hysteresis delay and said output loading adjustment.

138. (Previously Presented) The method of Claim 137 further comprising:

setting a hysteresis offset; and

generating one of said first or second output signals based on said first input signal, said second input signal, said hysteresis delay, said output loading adjustment and said hysteresis offset.

139. (Currently Amended) A method comprising:

setting a hysteresis offset;

setting a hysteresis delay; and

generating one of a first output signal or a second output signal based on ~~said~~ a first input signal, ~~said~~ a second input signal, said hysteresis offset and said hysteresis delay.

140. (Previously Presented) The method of Claim 139 further comprising:

setting an output loading adjustment; and

generating one of said first or second output signals based on said first input signal, said second input signal, said hysteresis offset, said hysteresis delay and said output loading adjustment.